Introduction

The purpose of this document is to define the format for the Kicad schematic symbol library files. This format supersedes the old file format defined in the file "library_file_format_EN.odt.

This file format is based on the Specctra DSN lexer[1] work graciously coded and contributed by Dick Hollenbeck. For those not familiar with the DSN format, it is very similar to the LISP programming language in that keywords are delimited by braces. It is also known as an S-expression format. A keyword may have zero or more tokens that behave like parameters for the keyword. Tokens may be defined as additional keywords creating a programming language like structure. The decision to change to this format is to provide a more robust file lexer, a human readable file format, better file error reporting, and improved extensibility. The other driving factor is to provide a more robust format for handling the various requirements of the component library developers.

Front Matter

This is a living document designed to be kept synchronized with the actual source code. If you modify the lexer, please update this specification as a courtesy to other developers. There are many third party tools that are used to generate, manipulate, and parse component library files. Keeping this document current is vital to developers of these tools.

Formatting

The DSN lexer enforces strict formatting requirements. Files must be encoded in UTF8 (ASCII) format. All lexer keywords are comprised of lower case letters, numbers, and underscores. Tokens may be any alphanumeric character delimited by a white space character. Each new delimited level of keywords is indented to make files easier to read and edit with a plain text editor. Comments are supported as separate lines indented at the same level as the current keyword delimiter and begin with the # character. In line comments are not allowed.

Using this document

This document is nothing more than several well commented part files. You should always be able to copy the text from the opening delimiter "(" to the closing delimiter ")" into a file and open it with the library part file editor or library part viewer in Kicad's schematic capture program EESchema. It may not actually draw a useful component or be a very useful part but it should always be syntactically correct. The comments for a specific keyword always appear above the keyword it describes. Keywords defined within brackets [] are optional. A simple syntax coloring scheme has been employed to make this document more readable. Keywords are highlighted in blue, comments are highlighted in turquoise, and strings are highlighted in red.

Logical coordinates.

The next version of EESchema and therefore the library parts will be based on either a 10nm or 100nm internal coordinate system. This will allow for 42.95 meter or 429.5 meter drawing space. The tool framework will allow the schematic editor to provide snapping to symbol pins. This guarantees all

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[1] See source files dsnlexer.cpp and dsnlexer.h in the Kicad source code for more information about how the DSN lexer works.

connectable items (pins, wires, junctions, etc.) will connected properly. The file format units will be in millimeters which is the same as the board and footprint library file formats.

Syntax for all drawable item types.

```
# File header:
# kicad_sym - defines the file as a kicad symbol library file.
# version - the version of the host program used to generate the symbol.
# host - the name and version of the host used to generate the symbol library file.
(kicad_sym  (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")

 # The symbol element is the root of the S expression used to define a library symbol.
 # Library symbols can be inherited from another symbol by using the extends keyword.
 # The symbol name is NAME where the name of the symbol is an escaped string.
 # Escaped strings will allow for more robust symbol names than using the file
 # name as the symbol name.  The optional power token defines if the symbol is a
 # a power symbol.  Required symbols defined in multiple unit symbol are required and should
 # be checked by the ERC. Symbols declared as atomic must follow the rules outlined in the
 # "Kicad Atomic Components" document and will be checked by the ERC accordingly.
 (symbol “NAME”  [power][required][atomic] [(extends “LPID”)][(uuid “UUID”)]

  # Change the anchor position to something other than 0, 0.
  [(anchor (at X Y))]

  # The reference property is required and reserved.  Optional reserved properties
  # are value, footprint, datasheet, and keywords.
  [(property “NAME” “VALUE”

   # Position requires an X and Y coordinates.  Angle is in degrees and defaults
   # to 0 if not defined.
   (at X Y [ANGLE])

   # Effects define how a property is displayed.  Effects can also be used to
   # override the effects of a property in an inherited symbol.  When used to
   # override the effects of an inherited property, the PROPERTY element must
   # be defined.
   [(effects

    # The FONT value needs to be defined.  Currently, EESchema does not support
    # different fonts.  In the future this feature may be implemented and at
    # that time FONT will have to be defined.  Initially, only the font size and
    # style are required.  Italic and bold styles are optional.  The font size
    # height and width are in units yet to be determined.
    (font [FONT] (size HEIGHT WIDTH) [ITALIC] [BOLD] [(color r g b a)])

    # Visible by default.
    [hide]
   )]
 ) # end symbol
```

```
# Shape objects combine multiple single drawing elements into a closed form
# that can optionally include a fill.  Missing segments where XY points do not overlap
# will be filled with a straight line segment that will be saved to the file on the next save
( shape

  # Valid fill types are filled and transparent.  No fill if undefined.
  # Fill colour defaults to the fill colour defined in the editor.
  [(fill FILL_TYPE) [(color r g b a)])]

  # The stroke width is required.  Line type defaults to solid when undefined.  The
  # supported line types are solid, dash, dot, and dash_dot.  More line types can be
  # added in future iterations.  The line color defaults to the line color defined in
  # the editor.
  [(stroke (width WIDTH) [(type LINE_TYPE)] [(color r g b a)])]

  # line, arc and bezier elements may be repeated here as many times as needed
  # When saving, Eeschema will begin with the upper left most point and continue to
  # the end of the element with the closest end point, stepping through the full compound object.
  # If the two elements share both endpoints, then which is used will be undefined.
  # The last xy coordinate listed in the compound object will be the same as the first xy coordinate.
  # Overlapping compound objects are allowed.
  [(line (pts (xy X Y) (xy X Y) ... )]

  # start and end are the two  end points of the arc
  # mid is a point on the circumference, half-way between start and end
  [(arc (start X Y) (mid X Y) (end X Y)  )]

  [(bezier (pts (xy X Y) (xy X Y) (xy X Y) (xy X Y) ) ]
)

# Either polyline or line can be used to define a line or series of lines.
# Coordinates can be non-integer.  The LINE_TYPE specifies the type of line such
# as dot, dot-dash, dash, etc.  No LINE_TYPE specifies a solid line.
(polyline or
(line
  (pts (xy X Y) (xy X Y) (xy X Y) (xy X Y) (xy X Y))

  # The line width is required.  Line type defaults to solid when undefined.
  # The line color defaults to the line color defined in the editor.
  [(width WIDTH)] [(type LINE_TYPE)] [(color r g b a)]
)

(circle
  (center X Y)

  # Radius length is in units if defined or mils.
  (radius LENGTH)
  [(stroke (width WIDTH) [(color r g b a)])]
  [(fill FILL_TYPE) [(color r g b a)])]
)
```

```
(arc (start X Y) (end X Y)  (radius LENGTH)
  [(width WIDTH)] [(color r g b a)]
)

(bezier
  (pts (xy X Y) (xy X Y) (xy X Y) (xy X Y) )
  [(width WIDTH)] [(color r g b a)]
)

(text “This is the text that gets drawn.”
  (at X Y [ANGLE])

  # Valid horizontal justification values are center, right, and left.
  # Valid vertical justification values are center, top, and bottom.  Default
  # justification is centered for both horizontal and vertical justification.
  [(effects
    (font [FONT] (size HEIGHT WIDTH) [ITALIC] [BOLD] [HORIZONTAL_JUSTIFY]
      [VERTICAL_JUSTIFY] [mirror] [(color r g b a)] [hide])]
    )
  )]
)

# A pin's type is its electrical connection.  Valid connection types are
# input, output, bidirectional, tristate, passive, unspecified, power_in,
# power_out, open_collector, open_drain, emitter_follower, sourc_follower
# unconnected.  Valid pin shape values are none, line, inverted, clock,
# inverted_clk, input_low, clock_low, falling_edge, and non_logic
# The optional SCOPE is used to specify if a pin label should be connects
# to all nets in a schematic by the pin name.  The only valid setting for
# SCOPE is “global”.  When SCOPE is not defined the connection is local to
# the pin connection point.
(pin TYPE SHAPE [SCOPE]

  # Pin coordinates must be integers.  The angle values 0, 180, 90, and 270
  # replace the current right, left, up, and down specifiers respectively.
  # No other angles are valid.
  (at X Y [ANGLE])

  # Length of the pin in units.  The pin length can be non-integer.  If no pin name
  # or pin number offset and/or angle is provided, the default pin name and number
  # offsets are used.
  (length LENGTH)
  (name “NAME” [(at X Y [ANGLE])]
    [(effects
      (font [FONT] (size HEIGHT WIDTH) [ITALIC] [BOLD] [(color r g b a)])
      [hide]
    )]
  )
  (number “NUMBER” [(at X Y [ANGLE])]
```

```
    [(effects
      (font [FONT] (size HEIGHT WIDTH) [ITALIC] [BOLD] [(color r g b a)])
      [hide]
    )]
   )
   (property "ATTRIBUTE_NAME" [ATTRIBUTE_VALUE]
   )
   [hide]

   # Alternate pin naming scheme allows a single pin to have a different name
   # pin type, and pin shape.  This allows for user to select a different pin
   # definition for symbols such as micro-controllers and FPGAs.  More than one
   # alternate is permitted.
   (alternate "ALT_NAME" TYPE SHAPE)
  )

  # Pin merge is used to group a number of pins that are connected to the same
  # point internally and shows the list or an ellipsized list of pins .  It is
  # typically used to hide power pins on symbols that have a large number of
  # power connections such as FPGAs and micro-controllers.
  # More than one pin_merge is permitted, but the same pin cannot be in more
  # than one pin_merge list.
  [(pin_merge "NUMBER1" "NUMBER2" ...)]

  # The pin swap hinting flag is used to indicate to an external tool ( i.e. an
  # auto router ) that the pins defined are functionally equivalent and
  # interchangeable.
  # More than one hint_pin_swap is permitted.
  [(hint_pin_swap "NUMBER1" "NUMBER2" ...)]
)
```

Syntax for Inheritance.

```
(symbol NAME_HINT (extends "LPID")

  # Remove pin NUMBER defined in the base symbol.  Only valid for extended symbols.
  [(pin_del "NUMBER")]

  # Swap pin NUMBER1 and pin NUMBER2 in the base symbol.  Only valid for extended
  # symbols.
  [(pin_swap "NUMBER1" "NUMBER2")]

  # Change the number of pin NUMBER1 to NUMBER2 in the base symbol.  Only valid
  # for extended symbols.
  [(pin_renum "NUMBER1" "NUMBER2")]

  # Change the name of pin NUMBER to NAME in the base symbol.  Only valid for
  # extended symbols.
  [(pin_rename "NUMBER" "NAME")]
```

```
  # Remove property NAME from the base symbol.  Only valid for extended symbols.
  # If NAME is omitted, all inherited properties will be removed.
  [(property_del [“NAME”])]

  # Alternates are used to define multiple symbol-per-package devices and/or
  # alternate body styles (DeMorgan).  Symbols must be defined in order.  There
  # can more than one alternate defined.
  [(alternate "LPID" ["LPID"...])]

  # Add a new property to this symbol.  Also can be use to override a property
  # defined in the base symbol.
  [(property “NAME” “VALUE”
    [(effects (at X Y [ANGLE])
      (font [FONT] (size HEIGHT WIDTH) [ITALIC] [BOLD])
      [hide]]
    )]

    # The alternates swap hinting flag is used to indicate to an external tool
    # that the symbols defined in the alternates list are functionally equivalent
    # and interchangeable.
    [(hint_alt_swap "LPID" "LPID" ...)]
  )
)
```

7400 Dual Input NAND Gate Sample

```
# This is an example of a dual input NAND gate A of a 7400.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
  (symbol “dual_input_nand_a”
    (reference “U”)
    (arc (pos 2 0) (radius 0.4) (start 2 -4) (start_angle -90) (end 2 4)
      (end_angle 90) (line_width 0) (fill none))
    (polyline (xy 2 4) (xy -6 4) (xy -6 -4) (xy 2 -4)
      (line_width 0) (fill none))
    (pin input line (at -12 2 180) (length 3.6)
      (name “” (font (size 1.2 1.2)) (visible yes))
      (number “1” (font (size 1.2 1.2)) (visible yes))
    )
    (pin input line (at -12 -2) (length 3.6)
      (name “” (font (size 1.2 1.2)) (visible yes))
      (number “2” (font (size 1.2 1.2)) (visible yes))
    )
    (pin output line (at -12 0)
      (name “” (font (size 1.2 1.2)) (visible yes))
      (number “3” (font (size 1.2 1.2)) (visible yes))
    )
    (pin power_in none (at -4 -4 90)
      (name “GND” (font (size 1.2 1.2)) (visible no))
```

```
    (number "7" (font (size 1.2 1.2)) (visible no))
    hide
   )
   (pin power_in none (at -4 4 90)
    (name "VCC" (font (size 1.2 1.2)) (visible no))
    (number "14" (font (size 1.2 1.2)) (visible no))
    hide
   )
   (hint_pin_swap "1" "2" )
  )
)

# All LPIDs below this point assume that the base symbol is located in the same
# library as the symbols that are derived from them.  See the "Distributed Library
# & EESchema Symbols List Design Documentation" in the Kicad source for more
# information on LPIDs.

# This is the B gate of a 7400.
(kicad_sym (version "20171130") (host "libedit" "5.0.0-rc2-147-g34c6393b7")
 (symbol "dual_input_nand_b" extends "dual_input_nand_a/rev1"
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 4)
  (pin_renum 2 5)
  (pin_renum 3 6)
 )
)

# This is the C gate of a 7400.
(kicad_sym (version "20171130") (host "libedit" "5.0.0-rc2-147-g34c6393b7")
 (symbol "dual_input_nand_c" extends "dual_in_nand_a/rev1"
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 9)
  (pin_renum 2 10)
  (pin_renum 3 8)
 )
)

# This is the D gate of a 7400.
(kicad_sym (version "20171130") (host "libedit" "5.0.0-rc2-147-g34c6393b7")
 (symbol "dual_input_nand_b" extends "dual_in_nand_a/rev1"
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 12)
  (pin_renum 2 13)
  (pin_renum 3 11)
 )
)
```

```
# This is a DeMorgan representation of a dual input NAND gate A.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
 (symbol “dual_input_nand_demorgan_a”
  (reference “U”)
  (arc (pos -9.3 0) (radius 0.518) (start -6 4) (start_angle 50.4)
   (end -6 -4) (end_angle -50.4) (line_width 0) (fill none))
  (arc (pos -0.22 2.86) (radius 7.06) (start 0 -200) (start_angle -88.1)
   (end 6 0) (end_angle -24.6) (line_width 0) (fill none))
  (arc (pos -0.2 2.82) (radius 6.8) (start 6 0) (start_angle -24.4) (end 0 4)
   (end_angle 88.3) (line_width 0) (fill none))
  (polyline (xy -6 4) (xy 0 4) (xy 0 -4) (xy -6 -4)
   (line_width 0) (fill none))
  (pin input line (at -12 2 180) (length 6)
   (name “” (font (size 1.2 1.2)) (visible yes))
   (number “1” (font (size 1.2 1.2)) (visible yes))
   (visible yes))
  (pin input line (at -12 -2 180) (length 6)
   (name “” (font (size 1.2 1.2)) (visible yes))
   (number “2” (font (size 1.2 1.2)) (visible yes))
   (visible yes))
  (pin output line (at -12 0) (length 7.4)
   (name “” (font (size 1.2 1.2)) (visible yes))
   (number “3” (font (size 1.2 1.2)) (visible yes))
   (visible yes))
  (pin power_in none (at -4 -4 90) (length 0)
   (name “GND” (font (size 1.2 1.2)) (visible no))
   (number “7” (font (size 1.2 1.2)) (visible no))
   (visible no))
  (pin power_in none (at -4 4 90) (length 0)
   (name “VCC” (font (size 1.2 1.2)) (visible no))
   (number “14” (font (size 1.2 1.2)) (visible no))
   (visible no))
  (hint_pin_swap 1 2)
 )
)

# This is the DeMorgan representation of gate B of a 7400.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
 (symbol “dual_input_nand_demorgan_b”
  extends “dual_in_nand_demorgan_a/rev1”
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 4)
  (pin_renum 2 5)
  (pin_renum 3 6)
  (pin_rename 1 “D”)
  (pin_rename 2 “E”)
  (pin_rename 3 “F”)
 )
)
```

```
# This is the DeMorgan representation of gate C of a 7400.
(kicad_sym “Dual Input NAND DeMorgan C” (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
(
 (symbol “dual_input_nand_demorgan_c”
  extends “dual_in_nand_demorgan_a/rev1”
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 8)
  (pin_renum 2 9)
  (pin_renum 3 10)
 )
)

# This is the DeMorgan representation of gate D of a 7400.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
 (symbol “dual_input_nand_demorgan_d”
  (extends “dual_in_nand_demorgan_a/rev1”)
  (pin_del 7)
  (pin_del 14)
  (pin_renum 1 11)
  (pin_renum 2 12)
  (pin_renum 3 13)
 )
)

# An example of putting it all together to create a 7400.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
 (symbol “quad_dual_input_nand_gate”
  (value “quad_dual_input_nand_gate”)
  (alternates
   “dual_in_nand_a/rev1”
   “dual_in_nand_b/rev1”
   “dual_in_nand_c/rev1”
   “dual_in_nand_d/rev1”
  )
  (alternates
   “dual_in_nand_demorgan_a/rev1”
   “dual_in_nand_demorgan_b/rev1”
   “dual_in_nand_demorgan_c/rev1”
   “dual_in_nand_demorgan_d/rev1”
  )
  (hint_alt_swap
   “dual_in_nand_a/rev1”
   “dual_in_nand_b/rev1”
   “dual_in_nand_c/rev1”
   “dual_in_nand_d/rev1”
  )
 )
)
```

```
# A 74LS00 is as simple as this.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
  (symbol “74LS00” (extends “quad_dual_input_nand_gate/rev1”) (value “74LS00”))
)

# This is a so called “atomic” or “fully defined” symbol definition of a Texas
# Instruments part number SN74HCT00NSR.
(kicad_sym (version “20171130”) (host “libedit” "5.0.0-rc2-147-g34c6393b7")
  (symbol “SN74HCT00NSR” atomic (extends “quad_dual_input_nand_gate/rev1”)
    (value “SN74HCT00NSR”)
    (footprint “14-SOP”)
    (datasheet “http://focus.ti.com/general/docs/lit/getliterature.tsp?genericPartNumber=sn74hct00&fileType=pdf”)
    (keywords “LOGIC” “NAND”)
    (property “Description” “IC GATE POS-NAND QD 2IN 14-SOP”)
    (property “Manufacturer” “Texas Instruments”)
    (property “Vendor” “Digikey”)
    (property “Vendor Part Number” “SN74HCT00NSR-ND”)
)
```